

Sub A1
1 1. A method comprising:
2 writing pixel data to a first memory location;
3 performing a first pixel transformation at said
4 first memory location;
5 generating a memory address for a second memory
6 location; and
7 writing said transformed pixel data from said
8 first memory location to said second memory location.

1 2. The method of claim 1 wherein writing pixel data
2 to a first memory location includes writing pixel data to a
3 first virtual memory location.

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1 3. The method of claim 2 further including writing
2 pixel data to a virtual memory location associated with a
3 memory controller client that receives pixel data written
4 to certain virtual addresses.

1 4. The method of claim 3 including causing an
2 operating system to set aside virtual addresses for said
3 memory controller client.

Sub A2
1 5. The method of claim 1 wherein entering an address
2 for a second memory location includes transforming the
3 addresses of said pixel data at said first memory location
4 to addresses at said second memory location.

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1 6. The method of claim 5 including determining the
2 offset to each pixel data by subtracting a base address at
3 said first memory location from the address of each pixel
4 data.

1 7. The method of claim 6 including adding said
2 offset to a base address of said second memory location.

1 8. The method of claim 1 wherein writing said
2 transformed pixel data from said first memory location to
3 said second memory location includes transferring said
4 pixel data to a memory controller using a memory controller
5 client.

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1 9. The method of claim 1 wherein writing said
2 transformed pixel data from said first memory location to
3 said second memory location includes writing said pixel
4 data from a first memory location associated with a first
5 transfer function to a second memory location associated
6 with a second transfer function.

1 10. The method of claim 9 including transforming the
2 addresses of said pixel data from addresses in a first
3 virtual memory range associated with said first transfer

4 function to memory addresses in a second virtual memory
5 range associated with said second transfer function.

1 11. An article comprising a medium storing
2 instructions that enable a processor-based system to:
3 write pixel data to a first memory location;
4 perform a first pixel transformation at said
5 first memory location;
6 generate a memory address for a second memory
7 location; and
8 write said transformed pixel data from said first
9 memory location to said second memory location.

1 12. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 write pixel data to a first virtual memory location.

1 13. The article of claim 12 further storing
2 instructions that enable the processor-based system to
3 write pixel data to a virtual memory location associated
4 with a memory controller client that receives pixel data
5 written to certain virtual addresses.

1 14. The article of claim 13 further storing
2 instructions that enable the processor-based system to

3 cause an operating system to set aside virtual addresses
4 for said memory controller client.

1 15. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 transform the addresses of pixel data at said first memory
4 location to addresses at said second memory location.

1 16. The article of claim 15 further storing
2 instructions that enable the processor-based system to
3 determine the offset to each pixel data by subtracting a
4 base address at said first memory location from the address
5 of each pixel data.

1 17. The article of claim 16 further storing
2 instructions that enable the processor-based system to add
3 said offset to a base address of said second memory
4 location.

1 18. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 transfer said pixel data to a memory controller using a
4 memory controller client.

1 19. The article of claim 11 further storing
2 instructions that enable the processor-based system to

3 write said pixel data from a first memory location
4 associated with a first transfer function to a second
5 memory location associated with a second transfer function.

1 20. The article of claim 19 further storing
2 instructions that enable the processor-based system to
3 transform the addresses of said pixel data from addresses
4 in a first virtual memory range associated with said first
5 transfer function to memory addresses in a second virtual
6 memory range associated with said second transfer function.

1 21. A system comprising:
2 a memory controller that receives pixel data and
3 addresses;
4 a first memory controller client that forwards
5 pixel data and addresses to a first transfer function; and
6 a second memory controller client that receives
7 data from said first transfer function together with new
8 addresses.

1 22. The system of claim 21 wherein said first
2 controller client selectively forwards pixel data and
3 addresses to one of a plurality of transfer functions and
4 said second controller client receives pixel data with new
5 addresses from a plurality of transfer functions.

